COMPLETE LISTING OF THE CLAIMS

The following lists all of the claims that are or were in the above-identified patent application. The status identifiers respectively provided in parentheses following the claim numbers indicate the current statuses of the claims. In particular, claims having the status of "currently amended" are being amended in this reply.

1. (Currently Amended) A process for testing a package containing a device, comprising:

bringing probe tips into contact with external terminals on the package;

using the probe tips to inelastically deform the external terminals to improve planarity of the external terminals; and

electrically testing the device through electrical connections of the probe ~~tip~~ tips to the external terminals.

2. (Original) The process of claim 1, wherein bringing the probe tips into contact with the external terminals comprises plugging the package into a socket.

3. (Original) The process of claim 2, wherein using the probe tips comprises applying pressure to the package while in the socket so that the probe tips deform the external terminals.

4. (Original) The process of claim 1, wherein each probe tip has a flat contact area and flattens a corresponding one of the external terminals, while simultaneously providing an electrical connection to the external terminals.

5. (Original) The process of claim 4, wherein the flat contact area has a width that is at least one half of a width of one of the terminals.

6. (Original) The process of claim 1, wherein the probe tips are affixed to a substrate.

7. (Original) The process of claim 6, wherein the substrate is a printed circuit board.

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8. (Original) The process of claim 7, wherein the probe tips comprise bonding pads disposed on a surface of the printed circuit board.

9. (Original) The process of claim 7, wherein the probe tips comprise bumps disposed on a surface of the printed circuit board.

10. (Original) The process of claim 1, wherein the probe tips are sized to accommodate relative thermal expansion of a pattern of the external terminals.

11. (Original) The process of claim 1, wherein the external terminals form a ball grid array.

12. (Currently Amended) A probing process comprising:

connecting a printed circuit board to test equipment, wherein the printed circuit board includes a set of contact pads having a pattern that matches elevated terminals on a package containing a device;

bringing the printed circuit board and the package into contact so that the elevated terminals on the ~~device~~ package make electrical connections with the contact pads on the printed circuit board; and

using the test equipment to test the device via the electrical connections of the printed circuit board to the package.

13. (Original) The process of claim 12, wherein the contact pads on the printed circuit board directly contact the elevated terminals of the package to make the electrical connections.

14. (Original) The process of claim 12, wherein the contact pads on the printed circuit board comprise bumps that directly contact the elevated terminals to make the electrical connections.

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15. (Original) The process of claim 12, wherein the elevated terminals comprise solder balls.

16. (Original) A package testing system comprising:

a substrate;

probe tips that are on the substrate and have flat contact surfaces;

a tester electrically connected to the probe tips; and

a mechanism capable of pressing external terminals of a package against the probe tips with sufficient force to inelastically deform the external terminals.

17. (Original) The system of claim 16, wherein each contact surface has a width that is at least one half of a width of a corresponding one of the external terminals.

18. (Original) The system of claim 16, wherein the substrate comprises a printed circuit board having contact pads in a pattern that matches a pattern of the external terminals of the package.

19. (Original) The system of claim 18, wherein the probe tips comprise the contact pads of a printed circuit board.

20. (Original) The system of claim 18, wherein the probe tips comprise bumps on the printed circuit board.

21. (Original) The system of claim 16, wherein the probe tips have sizes that accommodate relative thermal expansion of a pattern of the external terminals.

22. (New) The system of claim 16, wherein the mechanism is sized to accommodate a flip-chip package comprising a semiconductor device mounted on one side of a substrate, and the probe tips contact the external terminals that are on an opposite side of the substrate.

23. (New) The system of claim 16, wherein the flat contact surfaces of the probe tips are in a plane such that inelastic deformation caused by the mechanism pressing on the external terminals improves planarity of the external terminals.

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24. (New) The process of claim 1, wherein the package comprises a substrate having a first side on which the device is mounted and a second side on which the external terminals reside.

25. (New) The process of claim 24, wherein the package is a flip-chip package.

26. (New) The process of claim 12, wherein the package comprises a substrate having a first side on which the device is mounted and a second side on which the external terminals reside.

27. (New) The process of claim 26, wherein the package is a flip-chip package.

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